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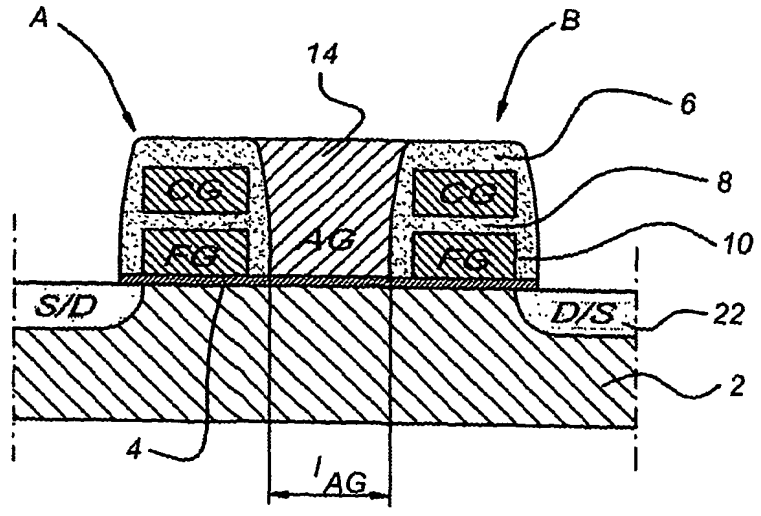
(54) Title: SELF-ALIGNED 2-BIT "DOUBLE POLY CMP" FLASH MEMORY CELL



(57) Abstract: Fabrication of a memory cell, the cell including a first floating gate stack (A), a second floating gate stack (B) and an intermediate access gate (AG), the floating gate stacks (A, B) including a first gate oxide (4), a floating gate (FG), a control gate (CG; CGl, CGu), an interpoly dielectric layer (8), a capping layer (6) and side-wall spacers (10), the cell further including source and drain contacts (22), wherein the fabrication includes: defining the floating gate stacks in the same processing steps to have equal heights; depositing over the floating gate stacks a poly-Si layer (12) with a larger thickness than the floating gate stacks' height; planarizing the poly-Si layer (12); defining the intermediate access gate (AG) in the planarized poly-Si layer (14) by means of an access gate masking step over the poly-Si layer between the floating gate stacks and a poly-Si etching step.

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